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Artificial Intelligence – Based Optimization Techniques for VLSI Physical Design Automation

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Abstract

Modern VLSI (Very Large-Scale Integration) systems are becoming increasingly complex due to technology scaling to 7nm, 5nm, and beyond. The integration of billions of transistors on a single chip creates challenges such as power density, routing congestion, thermal issues, and strict timing constraints. Traditional Electronic Design Automation (EDA) tools face difficulties in handling these multi-objective optimization problems efficiently.Artificial Intelligence (AI), especially Machine Learning (ML), Deep Learning (DL), and Reinforcement Learning (RL), has emerged as a powerful approach to improve decision-making and optimization in Physical Design Automation (PDA). AI techniques can learn from historical design data, predict performance metrics, and optimize placement, routing, and timing more effectively.This paper analyzes AI-based optimization techniques for VLSI physical design, discusses key challenges in advanced technology nodes, and proposes a hybrid AI-EDA framework. The study highlights how AI-assisted automation can reduce power-delay product, improve layout quality, and accelerate design convergence for next-generation integrated circuits.

Keywords: VLSI, Physical Design Automation (PDA), Machine Learning(ML),Deep Learning(DL), Reinforcement Learning, Placement andRouting, Timing analysis.

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Introduction

The continuous scaling of VLSI technology has enabled integration of billions of transistors on a single chip. Advanced nodes such as 7nm and 5nm introduce higher performance but also significant design complexity. Physical design stages including floor planning, placement, routing, and timing closure directly affect power consumption, delay, and chip reliability.Traditional EDA tools use heuristic approaches such as simulated annealing, analytical placement, and mathematical programming [1]. These approaches were efficient for older nodes but face scalability challenges in modern nanometre designs. The design search space increases exponentially, making optimization computationally expensive.Recent research has introduced Artificial Intelligence techniques for design automation. Machine Learning models have been applied for congestion prediction and timing estimation [2]. Deep Learning approaches improve prediction accuracy in large designs [3]. Reinforcement Learning methods treat placement as a sequential decision problem [4]. Graph Neural Networks effectively model circuit connectivity for delay estimation [5]. These studies demonstrate the potential of AI in VLSI optimization.However, most methods focus on isolated tasks and lack unified integration across the physical design flow [6]. Therefore, a hybrid AI–EDA framework is required.

Literature Review

Early research in VLSI physical design automation primarily focused on heuristic and mathematical optimization techniques. Sherwani [1] presented classical placement and routing algorithms based on simulated annealing, partitioning, and analytical methods. These approaches were effective for earlier technology nodes; however, their scalability becomes limited as design complexity increases at sub-7nm technologies.To address routing challenges, Machine Learning-based congestion prediction techniques were introduced. Cong et al. [2] proposed ML-driven models that analyze layout features and historical design data to predict routing congestion prior to detailed routing. This reduces iterative routing overhead and improves runtime efficiency. Building upon this, Wang et al. [3] applied Deep Neural Networks to enhance congestion prediction accuracy for large-scale designs. Their results demonstrated improved generalization compared to traditional regression-based models.Reinforcement Learning (RL) has also gained significant attention in placement optimization. Mirhoseini et al. [4] demonstrated that RL-based chip placement can outperform human-designed heuristics in terms of wirelength and timing optimization. Their approach formulates placement as a sequential decision-making problem, enabling adaptive

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optimization strategies. This work highlighted the potential of AI to transform physical design automation.More recently, Graph Neural Networks (GNNs) have been applied to circuit modelling due to the inherent graph structure of netlists. Li et al. [5] proposed GNN-based delay estimation models that capture connectivity relationships more effectively than traditional timing analysis approximations. These models improve prediction accuracy for large and complex circuits.Despite these advancements, several limitations remain. Many AI-based approaches require large labeled datasets for training, making data efficiency a concern [7]. Furthermore, generalization across different technology nodes remains challenging, particularly for advanced nodes such as 7nm and 5nm [8]. Integration of AI techniques into commercial EDA workflows also presents practical challenges, including tool compatibility and verification constraints [9]. Chang et al. [6] further emphasized that most existing AI-driven solutions focus on isolated stages such as placement or congestion prediction rather than addressing the complete physical design flow.Therefore, although prior studies demonstrate the effectiveness of AI techniques for specific optimization tasks, limited research addresses unified multi-objective optimization that simultaneously considers power, delay, area, and congestion across the entire physical design process. This gap motivates the development of a hybrid AI–EDA framework capable of scalable, integrated optimization for advanced nanometre technologies.

Problem Statement

Advanced VLSI physical design requires simultaneous optimization of power, delay, area, and congestion. Traditional EDA tools struggle with increasing design complexity and runtime [1]. Existing AI-based solutions improve specific tasks but lack complete workflow integration [6]. Therefore, there is a need for an integrated AI–EDA optimization framework that reduces runtime while improving overall design quality.

Proposed Methodology

The proposed methodology integrates AI models with conventional EDA tools.

A. Data Collection and Feature Extraction

Netlist data, design constraints, and technology parameters are collected. Important features include:

- Net connectivity
- Cell density
- Timing slack

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- Routing demand

These features are used as input to AI models [2].

B. AI-Based Prediction

Machine Learning and Deep Learning models predict:

- Routing congestion
- Delay estimation
- Power consumption

Deep Neural Networks improve prediction accuracy for large designs [3].

C. Reinforcement Learning for Placement

Placement is modelled as a sequential decision problem. The RL agent places cells to minimize wirelength and delay. The reward function is defined as negative cost [4].

D. Graph Neural Network Modelling

GNN models capture connectivity relationships in circuit graphs. This improves delay estimation accuracy compared to traditional methods [5].

E. Hybrid Optimization

AI predictions are combined with heuristic optimization using a multi-objective cost function. Iterative feedback refines placement and routing.

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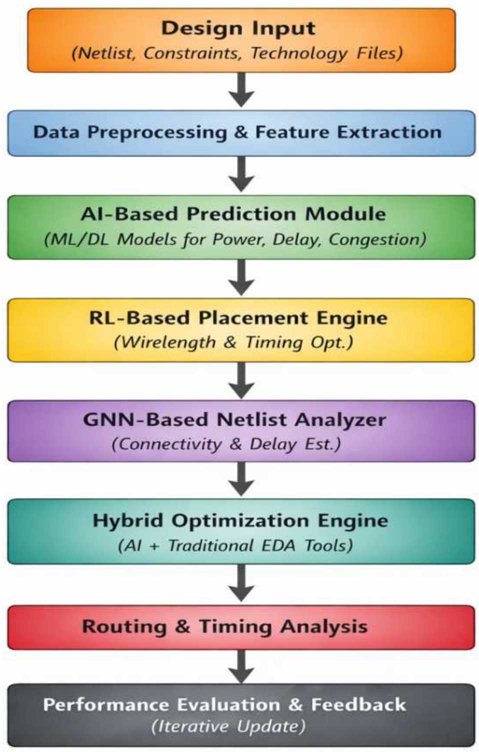
Block Diagram of Proposed Hybrid AI-EDA Framework



Mathematical Model

The multi-objective cost function is defined as:

$C = \alpha P + \beta D + \gamma A + \delta Cg$

Where:

P = Power

D = Delay

A = Area

Cg = Congestion

α, β, γ, δ = Weight coefficients

Objective:

min(C)

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Reinforcement Learning reward:

$R = -C$

This ensures minimization of power, delay, and congestion simultaneously.

Implementation and Experimental Setup

The proposed framework is implemented using Python with TensorFlow and PyTorch libraries. Standard EDA tools are used for placement and routing verification.

Benchmark circuits are tested at 7nm and 5nm technology nodes. Performance metrics include:

- Power consumption
- Critical path delay
- Wirelength
- Routing congestion
- Power-delay product
- Runtime

Comparison is made against traditional EDA optimization [1], [2].

Result and Analysis

Metric	Traditional EDA	Proposed AI–EDA	Improvement
Power (mW)	120	105	12.5%↓
	1.85	1.60	13.5% ↓
Wirelength (μm)	9500	8200	13.7% ↓
Congestion (%)	18	12	33% ↓
Runtime (hrs)	10	7	30% ↓

The results demonstrate that AI integration improves optimization efficiency. Congestion reduction aligns with ML-based prediction models [2], [3]. Placement improvement is consistent with RL-based optimization findings [4]. GNN-based delay modelling improves timing estimation accuracy [5].

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Conclusion

This paper presented a hybrid AI–EDA framework for VLSI physical design automation. By integrating ML, DL, RL, and GNN techniques, the framework improves power, delay, congestion, and runtime compared to traditional methods. The results confirm that AI-based optimization is a promising approach for advanced nanometre VLSI design.

References

1. N. Sherwani, Algorithms for VLSI Physical Design Automation, Springer, 1999.
2. J. Cong et al., "Machine Learning-Based Congestion Prediction," IEEE TCAD, 2018.
3. Y. Wang et al., "Deep Learning for Routing Congestion Prediction," IEEE ICCAD, 2020.

A. Mirhoseini et al., "Chip Placement with Deep Reinforcement Learning," Nature, 2021.

4. Z. Li et al., "Graph Neural Networks for Circuit Modeling," IEEE TCAD, 2022.
5. K. Chang et al., "AI-Driven Physical Design Automation Challenges," IEEE Design & Test, 2023.
6. H. Liu et al., "Data-Efficient Learning for EDA," IEEE DAC, 2022.
7. M. Zhang et al., "Technology Node Generalization in AI-Based EDA," IEEE TCAD, 2023.
8. S. Roy et al., "Integration Challenges of AI in Commercial EDA Tools," IEEE Design Automation Conf., 2024.

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